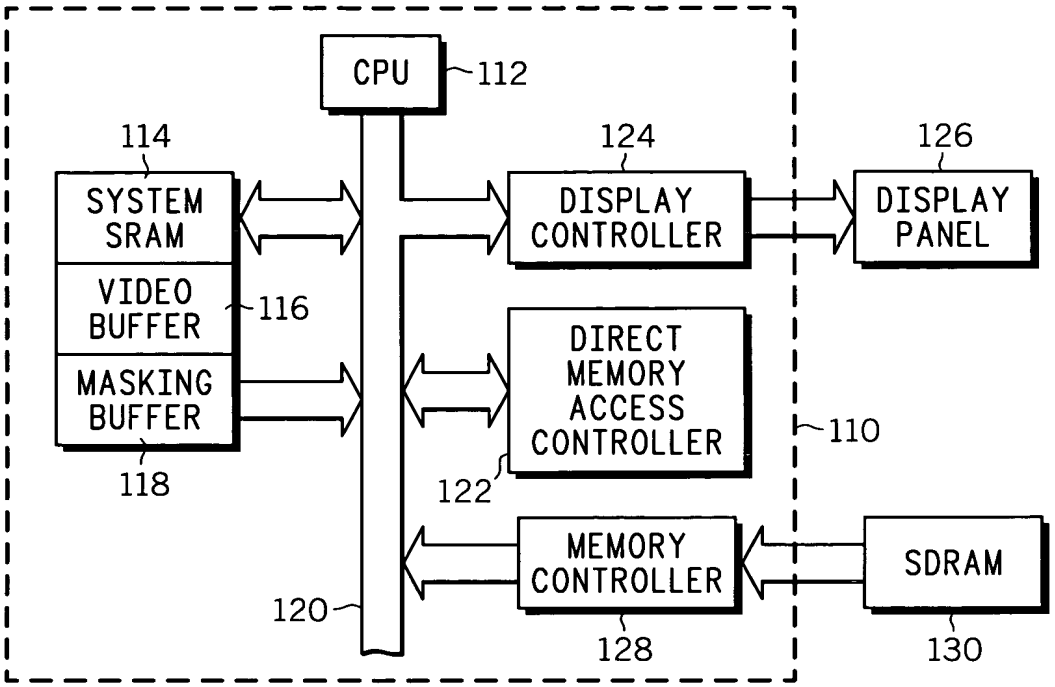
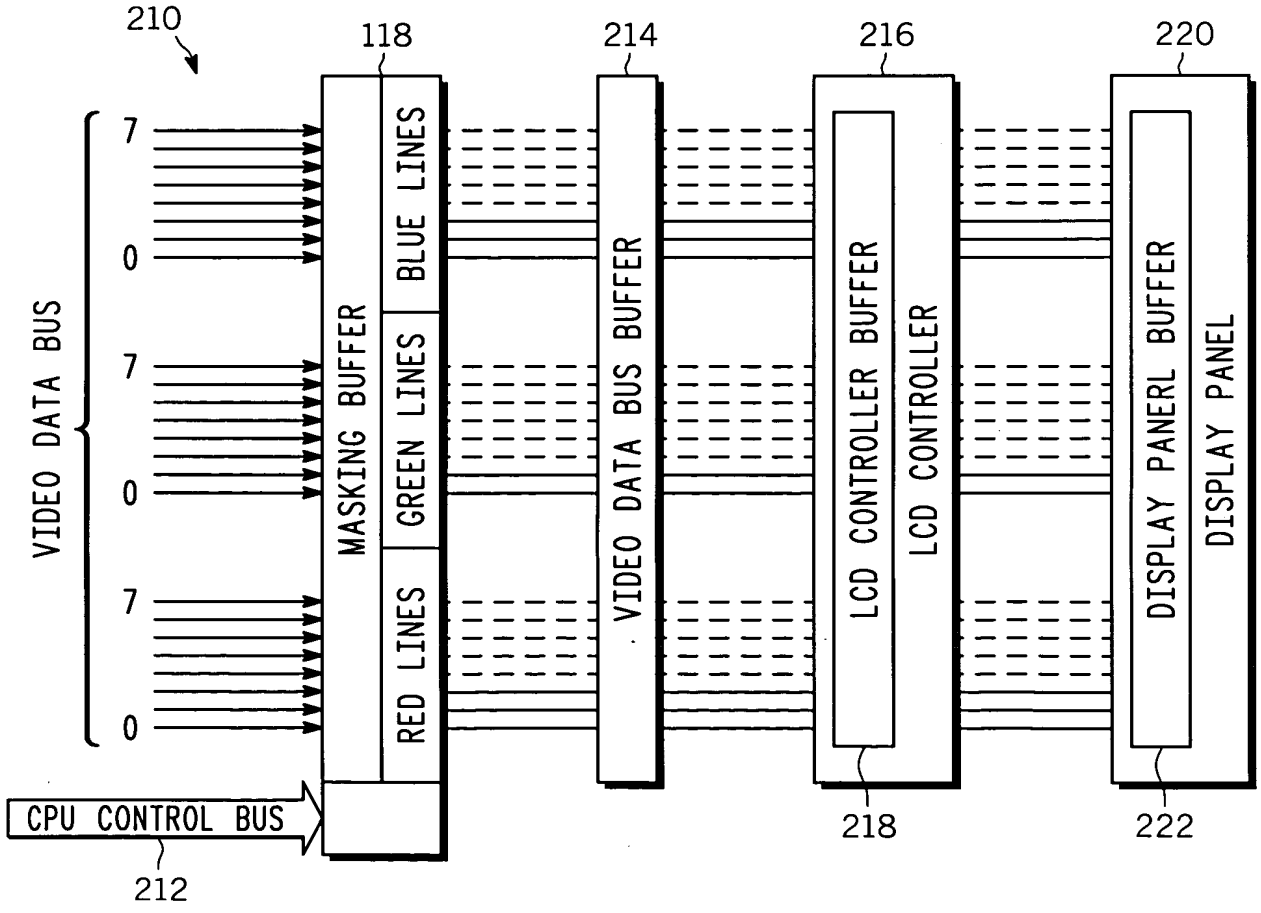


FIG. 1 108

FIG. 2



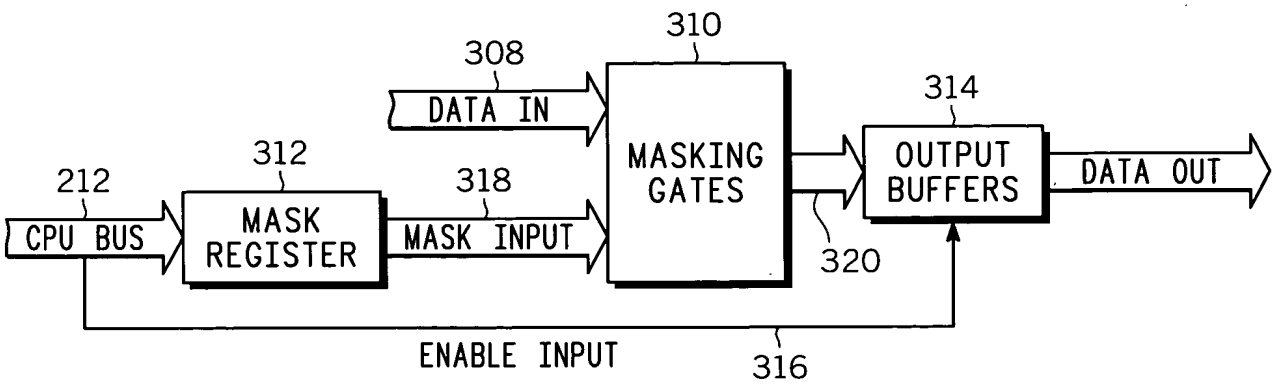


FIG. 3 118

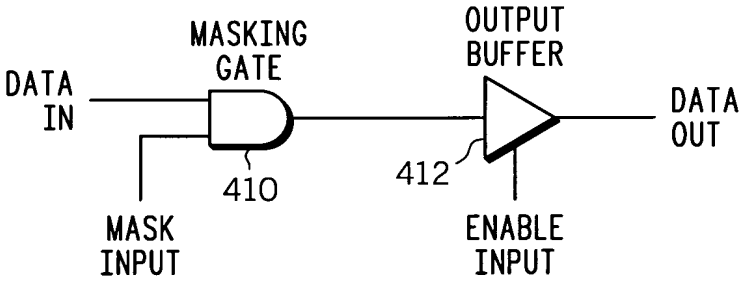


FIG. 4

FIG. 5

COLOR		BLUE								GREEN								RED							
LINE		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
GATED AND LOGIC	OUTPUT STATUS	0	0	0	0	0	X	X	X	0	0	0	0	0	0	X	X	0	0	0	0	0	X	X	X
	MASK REGISTER	0	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	1
GATED NAND LOGIC	OUTPUT STATUS	1	1	1	1	1	X	X	X	1	1	1	1	1	1	X	X	1	1	1	1	1	X	X	X
	MASK REGISTER	1	1	1	1	1	0	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	0	0	0

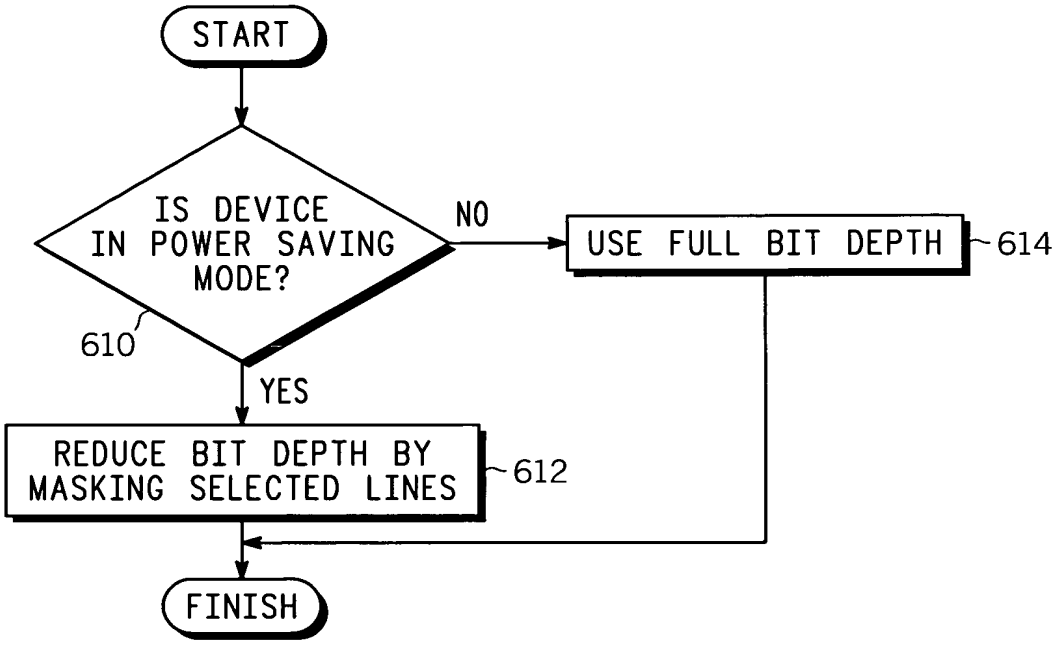
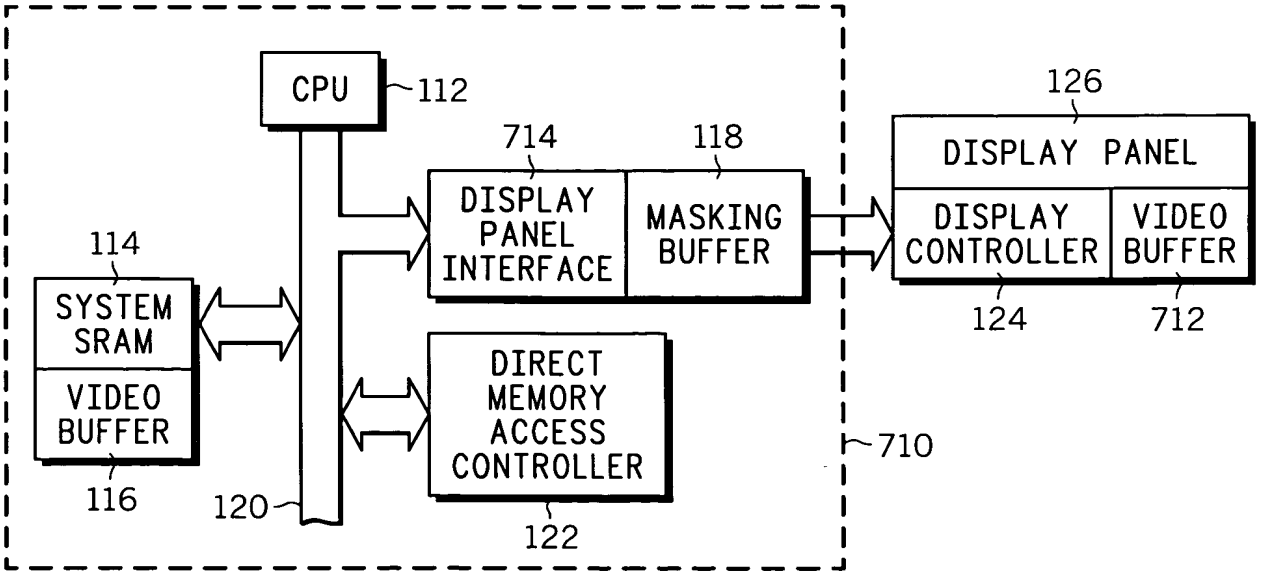


FIG. 6

708 FIG. 7



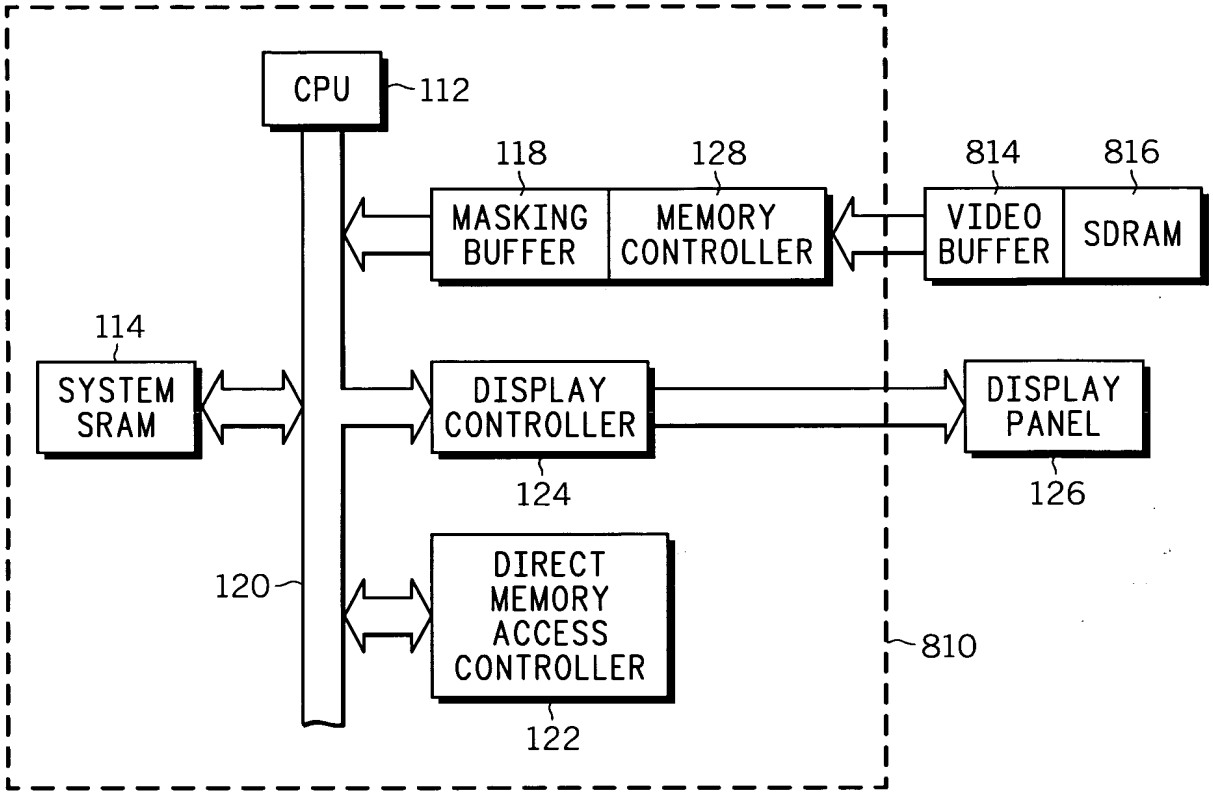


FIG. 8 808

908 FIG. 9